Technology Licensing Opportunity

UNIVERSITY OF SASKATCHEWAN

DECIMAL FLOATING POINT SQUARE-ROOT USING SRT ALGORITHM

Invention:

Given the popularity of decimal arithmetic, hardware implementation of decimal operations has been a hot topic in the recent decade. The square-root can be implemented as an instruction, directly in hardware, which improves performance of the decimal floating-point unit in the processors. This invention, with the intention of reducing the latency of the decimal square-root operation while maintaining a reasonable cost, proposes an SRT algorithm and the corresponding hardware architecture to compute the decimal square-root.

Decimal arithmetic is now finding merits and has need in various commercial and financial applications. The main reason for this growth is that decimal arithmetic can exactly mirror the human fractional computations while the binary arithmetic is not capable of doing so.

Decimal arithmetic has been very popular in the recent decades due to its human-centric applications and is supported by IEEE 754-2008 standard. Beside the popular four basic decimal operations (i.e., addition, subtraction, multiplication, and division), the square-root operation can be implemented as an instruction, directly in hardware. This boosts up the performance of the decimal floating-point unit in the processors.

Decimal Square-root computation is generally done in two ways:

- Multiplicative recurrence requires lower number of steps but each step is slow. This approach, using Newton-Raphson iterations, has higher cost.
- Additive recurrence takes more steps but each step is faster. In overall this approach is slower with lower cost.

Applications:

This has applications on the commercial and financial processors where all the computations are done based on the decimal number systems.

Advantages over existing Technology:

This invention is 16% faster than the state-of-the-art technology with about a quarter of the area. The main reason for this advantage lies within the fact that we have removed the slow and costly look-up tables from the design. Moreover, the SRT algorithm is used in this invention while previous works are based on Newton-Raphson iterations.

Main advantages of our hardware unit, over the previous works, are

- Removing slow and costly look-up tables
- Using additive approach to reduce the cost
- Modifying the additive approach to increase the speed
- Does not require any multiplier and is compatible with any decimal processor

As of 2014, the comparison results with the fastest previous work based on multiplicative recurrence, show that **our design is 16% faster and costs more than 4 times less**

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